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S. Minehane, R. Duane, P. O'Sullivan, K. G. McCarthy and A. Mathewson	1285	Design for reliability
T. G. Koetter, H. Wendrock, H. Schuehrer, C. Wenzel and K. Wetzig	1295	Relationship between microstructure and electromigration damage in unpassivated PVD copper damascene interconnects
H. Wendrock, W. Brückner, M. Hecker, T. G. Koetter and H. Schloerb	1301	Room temperature grain growth in electroplated copper thin films
R. Gonella, P. Motte and J. Torres	1305	Assessment of copper contamination impact on inter-level dielectric reliability performed with time-dependent-dielectric-breakdown tests

T. Berger, L. Arnaud, R. Gonella, G. Lormand and Y. Morand	1311	Electromigration characterization of damascene copper interconnects using normally and highly accelerated tests
A. Braghieri, I. De Munari, M. Impronta and A. Scorzoni	1317	Evaluation of the thermal resistance of Al-Cu electromigration test structures
V. Dattilo, B. Neri and C. Ciofi	1323	Low frequency noise evolution during lifetime tests of lines and vias subjected to electromigration
R. Gonella, J. Torres, P. Motte, E. van der Vegt and J. M. Gilet	1329	Impact of process steps on electrical and electromigration performances of copper interconnects in damascene architecture
D. Krüger, P. Gaworzewski, R. Kurps and K. Pomplun	1335	Influence of fluorine contamination on reliability of thin gate oxides
Z. Xu, B. J. Cho and M. F. Li	1341	Annealing behavior of gate oxide leakage current after quasi-breakdown
G. Cellere, A. Paccagnella, L. Pantisano, P. Colombo and M. G. Valentini	1347	Low-field latent plasma damage depassivation in thin-oxide MOS

TOPICS 3: FAULT LOCALISATION

		Invited Paper
M. K. Mc Manus, J. A. Kash, S. E. Steen, S. Polonsky, J. C. Tsang, D. R. Knebel and W. Huott	1353	PICA: Backside failure analysis of CMOS circuits using picosecond imaging circuit analysis
M. Litzenberger, K. Esmark, D. Pogany, C. Fürböck, H. Gossner, E. Gornik and W. Fichtner	1359	Study of triggering inhomogeneities in gg-nMOS ESD protection devices via thermal mapping using backside laser interferometry
C. Fürböck, K. Esmark, M. Litzenberger, D. Pogany, G. Groos, R. Zelsacher, M. Stecher and E. Gornik	1365	Thermal and free carrier concentration mapping during ESD event in smart power ESD protection devices using an improved laser interferometric technique
V. Pouget, P. Fouillat, D. Lewis, H. Lapuyade, F. Darracq and A. Touboul	1371	Laser cross section measurement for the evaluation of single-event effects in integrated circuits
K. Miura, K. Nakamae and H. Fujioka	1377	Automatic EB fault-tracing system using fuzzy-logic approach
R. Heiderhoff, M. Palaniappan, J. C. H. Phang and L. J. Balk	1383	Correlation of scanning thermal microscopy and near-field cathodoluminescence analyses on a blue GaN light emitting device
R. Weber, W. Mertin and E. Kubalek	1389	Voltage-influence of biased interconnection line on integrated circuit-internal current contrast measurements via magnetic force microscopy
P. Malberti, L. Ciampolini, M. Ciappa and W. Fichtner	1395	Quantification of scanning capacitance microscopy measurements for 2D dopant profiling
U. Behnke, W. Mertin and E. Kubalek	1401	Cross-talk in electric force microscopy testing of parallel submicrometer conducting lines
J. D'Haen, J. Van Olmen, Z. Beelen, J. V. Manca, T. Martens, W. De Ceuninck, M. d'Olieslaeger, L. De Schepper, M. Cannaerts and K. Maex	1407	In-situ SEM observation of electromigration in thin metal films at accelerated stress conditions

POSTER PAPERS

M. Zmeck, T. Osipowicz, F. Watt, F. Niedernostheide, H.-J. Schulze, G. B. M. Fiege and L. Balk	1413	Analysis of high-power devices using proton beam induced currents
R. Desplats, G. Rolland and P. Perdu	1419	Faster fault isolation using a dichotomy reduction of node candidates
F. Beaudoin, F. Saviot, D. Lewis, P. Perdu and F. Salin	1425	New non-destructive laser ablation based backside sample preparation method

P. Perdu, R. Desplats and F. Beaudoin	1431	A review of sample backside preparation techniques for VLSI
O. Mende and D. Niggemeyer	1437	Principle and application of a bifunctional laser linking and cutting structure for microelectronic circuits on standard CMOS-technology
Y. Haddab, V. Mosser, F. Kobbi and R. Pond	1443	Reliability and stability of GaAs-based pseudomorphic quantum wells for high-precision power metering
C. Sydlo, B. Mottet, M. Schüßler, M. Brandt and H. L. Hartnagel	1449	A method for HBT process control and defect detection using pulsed electrical stress
O. C. Khiam, B. J. Hua and S. Redkar	1455	Electrochemical wet etching in KOH:H_2O solution and secondary/ion image passive voltage contrast as a complementary technique in failure analysis
M. Catelani, M. Mugnaini and R. Singuaroli	1461	Effects of test sequences on the degradation analysis in high speed connectors
D. Pogany, K. Esmark, M. Litzenberger, C. Fürböck, H. Gossner and E. Gornik	1467	Bulk and surface degradation mode in 0.35 μm technology gg-nMOS ESD protection devices
P. Galy, V. Berland, B. Foucher, I. L-Valot, A. Guilhaume, J. P. Chante, S. Dufrenne and S. Bardy	1473	Numerical investigation for a grounded gate NMOS transistor under electrostatic discharge (ESD) through TLP method
H. W. Zan, P. S. Shih, T. C. Chang and C. Y. Chang	1479	Dimensional effects on the reliability of polycrystalline silicon thin-film transistors
B. Stadlober	1485	About long-term effects of hot-carrier stress on n-MOSFETS
D. Z. Peng, P. S. Shin, T. C. Chang and C. Y. Chang	1491	Reliability of passivated P-type polycrystalline silicon thin film transistors
J. L-Kwang, S. Ramey, J. M. Reynes, R. J. Hillard and T. Thieme	1497	The role of spreading resistance profiling in manufacturing control and technology development

TOPIC 4: PACKAGING, ASSEMBLIES AND RELIABILITY

P. Alpern, K. C. Lee, R. Dudek and R. Tilgner	1503	A simple model for the mode I popcorn effect for IC packages
S. Dilhaire, S. Jorez, A. Cornet, L. D. Patiño Lopez and W. Claeys	1509	Measurement of the thermomechanical strain of electronic devices by shearography
M. Petzold, L. Berthold, D. Katzer, H. Knoll, D. Memhard, and P. Meier, and K.-D. Lang	1515	Surface oxide films on aluminum bondpads: Influence on thermosonic wire bonding behavior and hardness
S. Ramminger, N. Seliger and G. Wachutka	1521	Reliability model for Al wire bonds subjected to heel crack failures
R. Rautioaho, O. Nousiainen, T. Saven, S. Leppävuori and J. Lenkkeri	1527	Thermal fatigue and metallurgical reactions in solder joints of LTCC modules
D. G. Yang, L. J. Ernst, C. van't Hof, M. S. Kiasat, J. Bisschop, J. Janssen, F. Kuper, Z. N. Liang, R. Schravendeel and G. Q. Zhang	1533	Vertical die crack stresses of flip chip induced in major package assembly processes
J. E. Semmens	1539	Flip chips and acoustic micro imaging: An overview of past applications present status, and roadmap for the future

TOPIC 5: SILICON DEVICES

		Invited Paper
R. S. Thewes, R. Brederlow, C. Schlüder, P. Wieczorek, B. Ankele, A. Hesener, J. Holz, S. Kessel and W. Weber	1545	MOS transistor reliability under analog operation
S. H. Hong, J. Y. Chun, C. G. Yu and J. T. Park	1555	The impacts of SILC and hot carrier induced drain leakage current on the refresh time in DRAM

G. Tao, A. Scarpa, J. Dijkstra, W. Stidl and F. Kuper 1561 Data retention prediction for modern floating gate non-volatile memories

J. M. Rafi and F. Campabadal 1567 Transconductance increase due to charge trapping during hot-carrier stress of nMOSFETs

H. Toutah, J. F. Llibre, B. T-Ighil, T. M-Brahim, K. Mourgues, Y. Helen, F. Raoult and O. Bonnaud 1573 Stability of polysilicon thin film transistors under switch operating

J. Kuchenbecker, M. Borgarino, A. Coustou, R. Plana, J. Graffeuil and F. Fantini 1579 Evaluation of the hot carrier/ionizing radiation induced effects on the RF characteristics of low-complexity SiGe heterojunction bipolar transistors by numerical simulation

L. Militaru, A. Souifi, M. Mouis and G. Brémond 1585 RTS noise in submicron SiGe epitaxial base bipolar transistors

J. W. McPherson, R. B. Khamankar and A. Shanware 1591 A complementary molecular-model (including field and current) for TDDB in SiO_2 dielectrics

E. Miranda and J. Suñé 1599 Modeling the conduction characteristics of broken down gate oxides in MOS structures

F. Crupi, G. Iannaccone, B. Neri, C. Ciofi and S. Lombardo 1605 Shot noise partial suppression in the SILC regime

S. J. Kim, B. J. Cho, P. F. Chong, E. F. Chor, C. H. Ang, C. H. Ling, M. S. Joo and I. S. Yeo 1609 Does short wavelength lithography process degrade the integrity of thin gate oxide?

TOPIC 6: PRODUCT REALISATION

R. C. Blish, II, J. C. Black, B. Hui and D. T. Prince 1615 Technique for determining a prudent voltage stress to improve product quality and reliability

J. C. Reiner, T. Keller, H. Jäggi and S. Mira 1619 Impact of ESD-induced soft drain junction damage on CMOS product lifetime

P. Miskowiec, D. Kunze and K. Lukat 1631 CALYPSO – Critical area, Lifetime, and Yield predicting software

M. Huber, Th. Nirschl, J. Gstöttner, M. Heinitz, Th. Zanon, W. Maly and D. S-Landsiedeal 1637 Yield and reliability analysis of digital standard cells with resistive defects

TOPIC 7: POWER DEVICES AND HIGH TEMPERATURE ELECTRONICS

G. Soelkner, J. Kreutle, J. Quincke, W. Kaindl and G. Wachutka 1643 Back side optical beam induced current method for the localization of electric field enhancements in edge termination structures of power semiconductor devices

C. Picard, C. Brisset, A. Hoffmann, J.-P. Charles, F. Joffre, L. Adams and A. H. Siedle 1649 Use of electrical stress and isochronal annealing on power MOSFETS in order to characterize the effects of ^{60}Co irradiation

M. H. Poech and R. Eisele 1655 A modelling approach to assess the creep behaviour of large-area solder joints

G. Lefranc, T. Licht, H. J. Schultz R. Beinert and G. Mitic 1661 Reliability testing of high-power multi-chip IGBT modules

G. Coquery and R. Lallemand 1667 Failure criteria for long term accelerated power cycling test linked to electrical turn off SOA on IGBT module. A 4000 hours test on 1200A-3300V module AlSiC base plate

Invited Paper

P. McCluskey, K. Mensah, C. O'Connor and A. Gallo 1673 Reliable use of commercial technology in high temperature environments

J. V. Manca, W. Wondrak, W. Schaper, K. Croes, J. D'Haen, W. De Ceuninck, B. Dieval, H. L. Hartnagel, M. D'Olieslaeger and L. De Schepper 1681 Reliability aspects of high temperature power MOSFETs

H. Ernst, E. Müller and W. A. Kaysser 1685 Thermal stability of laser welded thermocouple contacts to Si for high temperature thermal sensor application

J. Würfl, J. Hilsenbeck, E. Nebauer, G. Tränkle, H. Obloh and W. Österle 1691 Reliability of AlGaN/GaN HFETs comprising refractory ohmic and Schottky contacts

S. Forster, T. Lequeu, R. Jérisian and A. Hoffmann 1697 3-D analysis of the breakdown localised defects of ACS™ through a triac study

TOPIC 8: COMPOUND SEMICONDUCTORS

Invited Paper

D. Sauvage, D. Laffitte, J. Périnet, Ph. Berthier and J. L. Goudard 1703 Reliability of optoelectronic components for telecommunications

M. Dammann, M. Chertouk, W. Jantz, K. Köhler and G. Weimann 1711 Reliability of InAlAs/InGaAs HEMTs grown on GaAs substrate with metamorphic buffer

G. Meneghesso, R. Luise, D. Buttari, A. Chini, H. Yokoyama, T. Suemitsu and E. Zanomi 1717 Parasitic effects and long term stability of InP-based HEMTs

R. Petersen, W. De Ceuninck, L. De Schepper and J-L. Muraro 1723 A method to minimize test time for accelerated ageing of pHEMT's by analysis of the electronic fingerprint of the initial stage of degradation

B. Lambert, N. Saysset-Malbert, N. Labat, F. Verdier, A. Touboul, P. Huguet and F. Garat 1729 Comparison of RF and DC life-test effects on GaAs power MESFETs

M. Schüßler, B. Mottet, C. Sydlo, V. Krozer, H. L. Hartnagal and R. Jakoby 1735 Model for the decrease in HBT collector current under DC Stress based on recombination enhanced defect reactions

TOPIC 9: PHYSICAL FAILURE ANALYSIS

Invited Paper

G. Meneghesso, M. Ciappa, P. Malberti, L. Sponton, G. Croce, C. Contiero and E. Zanoni 1741 Overstress and electrostatic discharge in CMOS and BCD Integrated Circuits

H. J. Engelmann, H. Saage and E. Zschech 1749 Application of analytical TEM for failure analysis of semiconductor device structures

M. Vanzi, G. Salmini and R. De Palo 1755 New FIB/TEM evidence for a REDR mechanism in sudden failures of 980 nm SL SQW InGaAs/AlGaAs pump laser diodes

R. Desplats, T. Dargnies, J.-C. Courrege, P. Perdu and J.-L. Noullet 1761 Calculation of the optimal FIB milling and deposition operations for easier and faster circuit reconfiguration

N. Mattern, M. Hecker, D. Fischer, C. Wenzel, N. Schell, W. Matz, H. Engelmann and E. Zschech 1767 X-ray structure characterization of barriers for Cu metallization

NUMBER 11

C. C. Surya and H. Wong 1773 Editorial

I. THEORY AND MODELING

Invited Paper

B. Pellegrini 1775 A general model of $1/f$ noise

B. Kaulakys and T. Meškauskas 1781 Models for generation $1/f$ noise

B. Kaulakys 1787 On the intrinsic origin of $1/f$ noise

H. Ünlü 1791 Modeling of current transport and $1/f$ noise in heterojunction bipolar transistors

J. Kumičák 1799 Driven Lorentz gas with $1/f^{\alpha}$ *noise*

II. NANOMETER SCALE DEVICES

Invited Paper
A. Matulionis, V. Aninkevičius and J. Liberis 1803 Hot-electron velocity fluctuations in two-dimensional electron gas channels

Invited Paper
C. Claeys and E. Simoen 1815 Impact of advanced processing modules on the low-frequency noise performance of deep-submicron CMOS technologies

Invited Paper
Z. Çelik-Butler and F. Wang 1823 Effects of quantization on random telegraph signals observed in deep-submicron MOSFETs

Invited Paper
L. B. Kish and C. G. Granqvist 1833 Noise in nanotechnology

III. SILICON DEVICES

Invited Paper
J. E. Sanchez and G. Bosman 1839 Measurements of $1/f$ noise amplitude modulated by a large-signal carrier in bipolar junction transistors

Invited Paper
E. P. Vandamme and L. K. J. Vandamme 1847 Current crowding and its effect on $1/f$ noise and third harmonic distortion – a case study for quality assessment of resistors

Invited Paper
M. J. Deen and S. Rumyantsev 1855 Low frequency noise in complementary npn and pnp polysilicon emitter bipolar junction transistors

M. Sandén, B. G. Malm, J. V. Grahn and M. Östling 1863 Decreased low frequency noise by hydrogen passivation of polysilicon emitter bipolar transistors

C. Delseny, A. Pénarier, F. Pascal, S. G. Jarrix and P. Llinares 1869 Comparison of low frequency noise and high frequency performances of double and simple polysilicon Bi-CMOS BJT

N. V. Amarasinghe, Z. Çelik-Butler and P. Vasina 1875 Characterization of oxide traps in 0.15 μm^2 MOSFETs using random telegraph signals

F.-C. Hou, G. Bosman and M. E. Law 1883 Characterization of generation–recombination noise using a physics-based device noise simulator

D. Pogany, E. Gornik, M. Stecher and W. Werner 1887 Random telegraph noise and leakage current in smart power technology DMOS devices

A. Mercha, J. Rhayem, L. Pichon, M. Valenza, J. M. Routoure, R. Carin, O. Bonnaud and D. Rigaud 1891 Low-frequency noise in low temperature *unhydrogenated* polysilicon thin film transistors

IV. COMPOUND DEVICES

Invited Paper
J. A. Chroboczek and G. Ghibaudo 1897 Low frequency noise in SiGe-base heterojunction bipolar transistors and SiGe-channel metal oxide semiconductor field effect transistors

Invited Paper
C. Surya, C. F. Zhu, B. H. Leung, W. K. Fong, C. C. Cheng and J. K. O. Sin 1905 Study of the effects of rapid thermal annealing in generation–recombination noise in MBE grown GaN thin films

Invited Paper

J. Berntgen, A. Behres, J. Kluth, K. Heime, W. Daumann, U. Auer and F.-J. Tegude 1911 Hooge parameter of InGaAs bulk material and InGaAs 2DEG quantum well structures based on InP substrates

J. C. Vildeuil, M. Valenza and D. Rigaud 1915 Low frequency noise in gate and drain of PHEMT's and related correlation

M. Tacano, M. Ando, I. Shibasaki, S. Hashiguchi, J. Sikula and T. Matsui 1921 Dependence of Hooge parameter of InAs heterostructure on temperature

X. Y. Chen, A. Pedersen, O. G. Hellesø and A. D. van Rheenen 1925 Electrical noise of laser diodes measured over a wide range of bias currents

F. Principato and G. Ferrante 1929 Experimental determination of the kurtosis of RF noise in microwave low-noise devices

V. SYSTEMS AND INTERCONNECTIOIN

E. F. Tsakas and A. N. Birbas 1937 Noise optimisation for the design of a reliable high speed X-ray readout integrated circuit

K. Takagi, S. Serikawa and A. Okuno 1943 1/*f* phase noise in a transistor and its application to reduce the frequency fluctuation in an oscillator

T. González, J. Mateos, D. Pardo, O. M. Bulashenko and L. Reggiani 1951 Effect of dimensionality on shot-noise suppression in nondegenerate diffusive conductors

S. Di Pascoli and G. Iannaccone 1955 Simulation of electromigration noise in polycrystalline metal stripes

VI. MISCELLANEOUS

O. Marinov 1959 The low frequency noise in HFETs estimates the effect of electrical stress

A. Godoy, J. A. Jiménez-Tejada, A. Palma and J. E. Carceller 1965 Optimum design in a JFET for minimum generation–recombination noise

F. Principato and G. Ferrante 1969 Skewness and kurtosis of 1/*f* noise in semiconductor devices

J. Briaire and L. K. J. Vandamme 1975 The influence of a digital spectrum analyzer on the uncertainty in 1/*f* noise parameters

NUMBER 12

Introductory Invited Papers

K. P. Cheung 1981 Plasma-charging damage in ultra-thin gate oxide

Y. Wu, Q. Xiang, J. Y. M. Yang, G. Lucovsky and M.-R. Lin 1987 Time-dependent dielectric wearout technique with temperature effect for reliability test of ultrathin (<2.0 nm) single layer and dual layer gate oxides

V. V. Belyakov, A. I. Chumakov, A. Y. Nikiforov, V. S. Pershenkov, P. K. Skorobogatov and A. V. Sogoyan 1997 IC's radiation effects modeling and estimation

Research Papers

C. Lee, J.-S. Kim, H. Shin, Y.-J. Park and H.-S. Min 2019 A new hole mobility model for hydrodynamic simulation

A. A. Tarasenko, F. Nieto, L. Jastrabik and C. Uebing 2023 The influence of adatom diffusion on coverage and emission current fluctuations

A. Paskaleva and E. Atanassova 2033 Bulk oxide charge and slow states in Si–SiO_2 structures generated by RIE-mode plasma

B.-Y. Tsui, S.-S. Lin, C.-S. Tsai and C. C. Hsia 2039 Plasma charging damage during contact hole etch in high-density plasma etcher

S. Oussalah, F. Nebel and R. Jérisian	2047	On the optimum thickness to test dielectric reliability, in an integrated technology of power devices
T. M. Korhonen, D. D. Brown and M. A. Korhonen	2053	A grain structure based statistical simulation of electromigration damage in chip level interconnect lines
G. Boselli, T. Mouthaan and F. Kuper	2061	Rise-time effects in grounded gate nMOS transistors under transmission line pulse stress
G. Hanreich, J. Nicolics and L. Musiejovsky	2069	High resolution thermal simulation of electronic components
M. Amagai	2077	The effect of polyimide surface chemistry and morphology on critical stress intensity factor
I. V. Vasiltsov and B. A. Mandziy	2087	Estimation of the reliability of digital systems implemented on programmable devices
A. A. Ismaeel, R. Bhatnagar and R. Mathew	2095	Concurrent testing in high level synthesis
		Research Notes
A. Srivastava	2107	Back gate bias method of threshold voltage control for the design of low voltage CMOS ternary logic circuits
A. Srivastava	2111	Total dose response studies of n-channel SOI MOSFETs for low power CMOS circuits
D. Moore and A. S. Papadopoulos	2117	The Burr type XII distribution as a failure model under various loss functions
L. Qi, J. Shi, H. Li, E. Jin and D. Gao	2123	The peaks in the electric derivative curves and optic derivative curves of GaAs/GaAlAs high-power QW lasers
	2129	Book review